UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,678	05/04/2006	Kazuki Noda	59018US007	4637

32692 7590 11/16/2009

3M INNOVATIVE PROPERTIES COMPANY
PO BOX 33427
ST. PAUL, MN 55133-3427

EXAMINER	
HENRY, CALEB E	

ART UNIT	PAPER NUMBER
2894	

NOTIFICATION DATE	DELIVERY MODE
11/16/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

LegalUSDocketing@mmm.com
LegalDocketing@mmm.com

Office Action Summary	Application No.	Applicant(s)	
	10/595,678	NODA, KAZUKI	
	Examiner	Art Unit	
	CALEB HENRY	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 2-3, filed 07/14/2009, with respect to claim 1-3 have been fully considered and are persuasive. The finality has been withdrawn.

2. However, upon further consideration, a new ground(s) of rejection has been made below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oka (US 6551906 B2), in view of Fan (5300788).

Regarding claim 1, Oka teaches a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 3, lines 35-49), comprising (Figure 1A-1C):

joining the circuit side (front surface [surface at which semiconductors elements are found], col. 3, lines 35-49) of said semiconductor wafer (wafer, 1) to a polymeric film material (tape substrate, 21) via a fluid surface protecting layer (adhesive, 22), and

grinding said wafer (Oka, col. 3, lines 35-49), wherein grinding said wafer is done after hardening said surface protecting layer (Oka, col. 3, lines 35-49).

Oka does not teach that the UV resin hardens upon radiation exposure.

Fan teaches a UV curable epoxy which hardens when exposed to UV light (Fan, col. 11, lines 3-21).

Fan teaches that the use of such an epoxy allows for selectively transforming the material to a solid state and removing the material leftover which has not been transformed (Fan, col. 11, lines 3-21). Thus, certain areas can be masked.

It would have been obvious to one with ordinary skill in the art at the time of the invention to append the teachings of Fan to the teachings of Oka, due to aforementioned reasons.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oka (US 6551906 B2), in view of Fan (5300788), in view of Morita (5516858).

Regarding claim 2, Oka teaches a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding (Oka, col. 3, lines 35-49) of the wafer (Oka, fig. 1A-1C, 1), comprising:

providing a surface protecting sheet (Oka, figs. 1A-1C, 2) comprising a polymeric film material (Oka, figs. 1A-1C, 21) on which is a surface protecting layer (Oka, figs. 1A-1C, 22) which becomes fluid upon heating [the term “heating” has many connotations for various materials. Thus, a material could be heated by merely placing it at room temperature]

heating said surface protecting sheet to make the surface protecting layer effectively fluid [the term “heating” has many connotations for various materials. Thus, a material could be heated by merely placing it at room temperature],

placing the circuit side of said semiconductor wafer in contact with the fluidized surface protecting layer (Oka, figs. 1A-1C),

hardening said surface protecting layer (Oka, col. 3, lines 35-49), and

grinding said wafer, wherein grinding said wafer is done after hardening said surface protecting layer (Oka, col. 3, lines 35-49).

Oka does not teach a layer which hardens upon exposure to radiation or upon heating to a temperature higher than the fluidizing temperature.

Oka does not teach the surface protecting sheet having a polymeric film material which is solid at room temperature

Fan teaches a UV curable epoxy which hardens when exposed to UV light (Fan, col. 11, lines 3-21).

Fan teaches that the use of such an epoxy allows for selectively transforming the material to a solid state and removing the material leftover which has not been transformed (Fan, col. 11, lines 3-21). Thus, certain areas can be masked.

Also, one with common knowledge in the art would know that in order to "harden", it would had have to have been more fluid than it once was. Thus, in order for the UV curing resin to harden upon exposure to UV light, it would have had to have been fluid.

Morita teaches a curable resin, used for protective coatings, with a main component (component A) which can be a UV-curing resin which may be a liquid or a solid at room temperature (Morita, col. 3, lines 51-57).

Oka, Fan and Morita teach of resins pertaining to the same field of endeavor i.e. protection of electrical elements (Morita, col. 2, lines 15-32). Also, the addition of such a curing resin, to the teachings of Oka would allow for greater versatility, since it can be in either a liquid or solid state at room temperature (Morita, col. 3, lines 56-57). Also, Morita teaches that this curable resin has excellent flexibility, moisture resistance, and heat shook resistance, of which are of great value in the semiconductor art (Morita, col. 2, lines 40-52).

Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Morita and Fan to the teachings of Oka due to aforementioned reason(s).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oka (US 6551906 B2), in view of Fan (5300788), in view of Morita (5516858).

Regarding claim 3, Oka teaches a surface protecting sheet for protection of the circuit side of a semiconductor wafer during the step of back side grinding of the wafer (Oka, col. 3, lines 35-49), the surface protecting sheet (Oka, fig. 1A-1C, 2) comprising a polymeric film material (Oka, fig. 1A-1C, 21) on which is formed a surface protecting layer (Oka, fig. 1A-1C, 22) which becomes fluid upon heating (the term “heating” has many connotations for various materials. Thus, a material could be heated by merely placing it at room temperature) and hardening the layer (Oka, col. 3, lines 35-49).

Oka does not teach which is solid at room temperature and hardening upon exposure to radiation or upon heating to a temperature higher than the fluidizing temperature.

Morita teaches a curable resin, used as a protective coating in electronic elements, with a main component (component A) which can be a UV-curing resin which may be a liquid or a solid at room temperature (Morita, col. 3, lines 51-57).

Oka and Morita teach of resins pertaining to the same field of endeavor i.e. protection of electrical elements (Morita, col. 2, lines 15-32). Also, the addition of such a curing resin, to the teachings of Oka would allow for greater versatility, since it can be in either a liquid or solid state at room temperature (Morita, col. 3, lines 56-57). Also, Morita teaches that this curable resin has excellent flexibility, moisture resistance, and heat shook resistance, of which are of great value in the semiconductor art (Morita, col. 2, lines 40-52).

Fan teaches a UV curable epoxy which hardens when exposed to UV light (Fan, col. 11, lines 3-21).

Fan teaches that the use of such an epoxy allows for selectively transforming the material to a solid state and removing the material leftover which has not been transformed (Fan, col. 11, lines 3-21). Thus, certain areas can be masked.

Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Morita and Fan to the teachings of Oka due to aforementioned reason(s).

7. Claims 4-6, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oka/Morita/Fan as applied to claim 3 above, and further in view of Hosomi (5726219).

Regarding claim 4, Oka/Fan, in view of Morita, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Fan, in view of Morita, does not teach a surface protecting sheet according to claim 3, wherein, before hardening of the surface protective layer, the protective layer has an elastic shear loss modulus (G") less than its elastic shear storage modulus (G') at room temperature (20-25°C) and an elastic shear loss modulus (G") greater than its elastic shear storage modulus (G') at 30-100°C, as measured with a viscoelesticity measuring apparatus at a frequency of 10 Hz, a deformation of 0.04% and a temperature ramp rate of 3 °C/rain., and the surface protective layer after hardening has an elastic tensile storage modulus (E') at 50°C greater than 5 x 107 Pa as measured with a viscoelesticity measuring apparatus at a frequency of 1 Hz, a deformation of 0.04% and a temperature-ramp rate of 5°C/min.

Hosomi teaches a resin which contains the components necessary to form phenol-novolac epoxy (meth)acrylate resin (Hosomi, col. 2, lines 25 -50, (b)). Since phenol-novolac epoxy (meth)acrylate resin is one of the main materials that can be utilized as the in the surface protecting layer, it must have the characteristics laid out in claim 4.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Hosomi to the teachings of the Oka/Fan/Morita combination because phenol-novolac epoxy (meth)acrylate resin offers heat resistance at temperatures as high as 260 degrees Celsius.

Regarding claim 5, Oka/Fan, in view of Morita, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Fan, in view of Morita, does not teach a surface protecting sheet according to claim 3, wherein the surface protecting layer contains at least one type of a free-radical polymerizable compound having two or more ethylenically unsaturated moieties in the molecule, the free-radical polymerizable compound being:
(3) the following resins having a molecular weight of 1000 or greater which are solid at room temperature (20-25°C): phenol-novolac epoxy (meth)acrylate resins.

Hosomi teaches a resin which contains the components necessary to form phenol-novolac epoxy (meth)acrylate resin (Hosomi, col. 2, lines 25 -50, (b)).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Hosomi to the teachings of the Oka/Fan/Morita combination because phenol-novolac epoxy (meth)acrylate resin offers heat resistance at temperatures as high as 260 degrees Celsius.

Regarding claim 6, Oka/Fan, in view of Morita, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Fan, in view of Morita, does not teach the use of a free-radical polymerization initiator.

Hosomi teaches the use of a free-radical polymerization initiator (photopolymerization initiator) (Hosomi, col. 2, lines 55-65, (e)).

Free-radical polymerization initiators are needed in UV curing resin in order to initiate polymerization reaction.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Hosomi to the teachings of the Oka/Fan/Morita combination because UV curing resins generally need a free-radical polymerization initiator in order for the UV light to have its intended effect.

Regarding claim 9, Oka/Fan, in view of Morita, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Fan, in view of Morita, does not teach a surface protecting sheet according to claim 3, wherein the surface protecting layer contains at least one type of a free-radical polymerizable compound having two or more ethylenically unsaturated moieties in the molecule, the free-radical polymerizable compound being:
(3) the following resins having a molecular weight of 1000 or greater which are solid at room temperature (20-25°C): phenol-novolac epoxy (meth)acrylate resins.

Hosomi teaches a resin which contains the components necessary to form phenol-novolac epoxy (meth)acrylate resin (Hosomi, col. 2, lines 25 -50, (b)).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Hosomi to the teachings of the Oka/Fan/Morita combination because phenol-novolac epoxy (meth)acrylate resin offers heat resistance at temperatures as high as 260 degrees Celsius.

Regarding claim 10, Oka/Fan, in view of Morita, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Fan, in view of Morita, does not teach the use of a free-radical polymerization initiator.

Hosomi teaches the use of a free-radical polymerization initiator (photopolymerization initiator) (Hosomi, col. 2, lines 55-65, (e)).

Free-radical polymerization initiators are needed in UV curing resin in order to initiate polymerization reaction.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Hosomi to the teachings of the Oka/Fan/Morita combination because UV curing resins generally need a free-radical polymerization initiator in order for the UV light to have its intended effect.

8. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oka/Morita/Fan as applied to claim 3 above, and further in view of Komiyama (5118567).

Regarding claim 7, Oka/Fan, in view of Morita, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Fan, in view of Morita, does not teach a surface protecting sheet according to claim 3 wherein the surface protecting layer contains at least one cationically polymerizable compound having two or more cationically polymerizable groups in the

molecule, the cationically polymerizable compound being:

(2) phenol-novolac epoxy resins of molecular weight 1000 or greater which are solid at room temperature.

Komiyama teaches the use of an adhesive tape which is composed of phenol-novolac epoxy resin (Komiyama, col. 3, lines 57-67). This adhesive tape has adhesive/releasing properties which are well balanced, which initially was a problem in prior art (Komiyama, col. 1, lines 30-36).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Komiyama to the teachings of the Oka/Fan/Morita combination because it offers a balance between adhesive and releasing properties.

Regarding claim 8, Oka/Fan, in view of Morita, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Fan, in view of Morita, does not teach the use of a free-radical polymerization initiator.

Komiyama teaches the use of a cationic polymerization initiator (photopolymerization initiator) (Komiyama, col. 2, lines 1-12).

Cationic polymerization initiators are needed in UV curing resin in order to initiate polymerization reaction.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Komiyama to the teachings of the

Oka/Fan/Morita combination because UV curing resins generally need a free-radical polymerization initiator in order for the UV light to have its intended effect.

9. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oka/Morita/Fan/Hosomi as applied to claim 4 above, and further in view of Komiyama (5118567).

Regarding claim 11 Oka/Fan/Morita/Hosomi teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Fan/Morita/Hosomi do not teach a surface protecting sheet according to claim 3 wherein the surface protecting layer contains at least one cationically polymerizable compound having two or more cationically polymerizable groups in the molecule, the cationically polymerizable compound being:
(2) phenol-novolac epoxy resins of molecular weight 1000 or greater which are solid at room temperature.

Komiyama teaches the use of an adhesive tape which is composed of phenol-novolac epoxy resin (Komiyama, col. 3, lines 57-67). This adhesive tape has adhesive/releasing properties which are well balanced, which initially was a problem in prior art (Komiyama, col. 1, lines 30-36).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Komiyama to the teachings of the Oka/Fan/Morita/Hosomi combination because it offers a balance between adhesive and releasing properties.

Regarding claim 12, Oka/Fan/Morita/Hosomi teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Fan/Morita/Hosomi does not teach the use of a free-radical polymerization initiator.

Komiyama teaches the use of a cationic polymerization initiator (photopolymerization initiator) (Komiyama, col. 2, lines 1-12).

Cationic polymerization initiators are needed in UV curing resin in order to initiate polymerization reaction.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Komiyama to the teachings of the Oka/Fan/Morita/Hosomi combination because UV curing resins generally need a free-radical polymerization initiator in order for the UV light to have its intended effect.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CALEB HENRY whose telephone number is (571)270-5370. The examiner can normally be reached on Monday-Thursday, 7:30 AM- 5:30 PM, ALT. Fridays, Est..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly D. Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CALEB HENRY/
Examiner, Art Unit 2894

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894